AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-10. (Cancelled)

11. (Previously Presented) A circuit comprising:

a first terminal of an integrated circuit (IC) coupled to receive power for on-die combinational circuitry when the integrated circuit is in an active mode and to not receive power when the integrated circuit is in a low power mode;

a second terminal to receive power supplied to circuitry for low power logical state retention of the IC when the integrated circuit is in the low power mode, wherein the second terminal provides power to low-leakage memory that stores the logical state; and

a multiplexer to receive a signal from an internal portion of the integrated circuit and a signal external to the integrated circuit, where an output of the multiplexer is coupled to a power regulator.

12. (Original) The circuit of claim 11 further comprising:

a transistor external to the integrated circuit to gate the power received at the first terminal.

13. (Original) The circuit of claim 12, wherein the transistor is coupled to a power regulator and switched off when the integrated circuit is in the low power mode.

14. (Original) The circuit of claim 11 wherein a feedback signal is taken from the first terminal and supplied to a power regulator.

15. (Original) The circuit of claim 11 wherein a feedback signal is taken from within the integrated circuit and supplied to a power regulator.

16. (Cancelled)

17. (Original) The circuit of claim 11 further comprising:

a transistor internal to the integrated circuit to gate the power received at the first terminal and float an internal power conductor connected to combinational logic.

18. (Previously Presented) A system comprising:

an integrated circuit having a power terminal coupled through an external control transistor to an output of a power supply; and

a multiplexer that selectively connects an external power signal supplied at a pin of the integrated circuit, an internal power signal of the integrated circuit, and a power signal supplied to the external control transistor to the power supply.

19. (Original) The system of claim 18 wherein the control transistor is an NMOS transistor.

20. (Original) The system of claim 18 wherein the control transistor is a CMOS pass gate.

21. (Cancelled)

22. (Previously Presented) The system of claim 18 wherein the multiplexer disconnects the power signal from the power supply while the integrated circuit is in a low power standby mode.